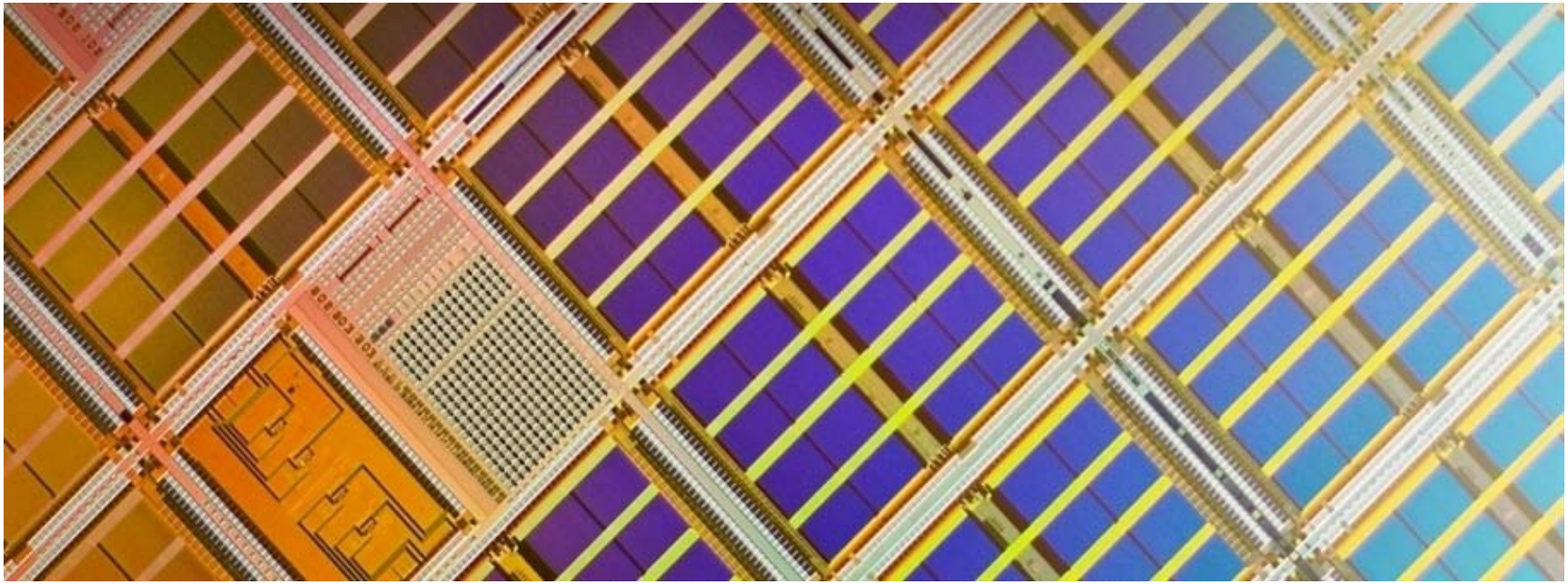


Status and Prospect for MRAM Technology

Dr. Saied Tehrani

Nonvolatile Memory Seminar

Hot Chips Conference

August 22, 2010

Memorial Auditorium

Stanford University

Everspin Technologies, Inc. - © 2010

EVERSPIN TECHNOLOGIES

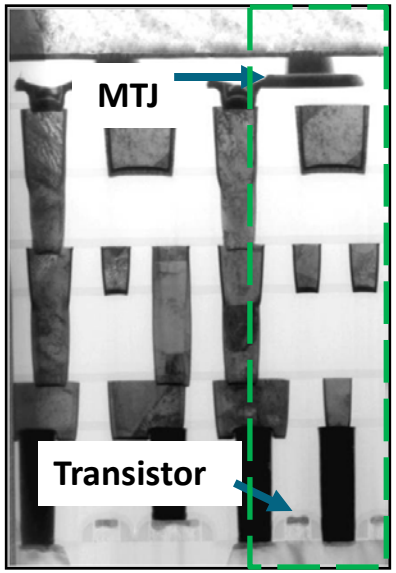
Agenda

- Current status of MRAM products
- MRAM features
- Current MRAM product operation
- Recent advancement in MRAM technology
- Prospect for MRAM

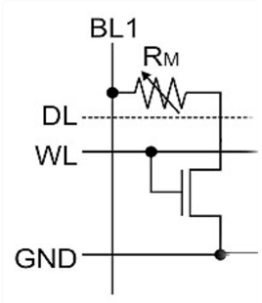
Everspin Introduction

- **Formed as Everspin in June 2008 – Previously part of Freescale Semiconductor**
- **The leading developer and manufacturer of integrated magnetic products**
  - Industry-first MRAM supplier since June 2006
  - Embedded MRAM systems
  - Integrated magnetic sensors
- **Current MRAM products**
  - Parallel interface products ranging from 256k-16Mb
    - Infinite endurance, >20 year data retention, 35 ns read & write speed
  - Serial interface products ranging from 256kb-1Mb
    - 40 MHz SPI interface, No write delay, infinite endurance

Everspin MRAM Technology

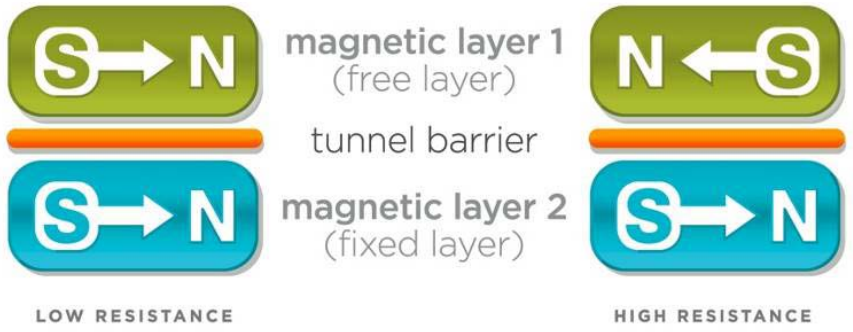


Cross-sectional view



Circuit

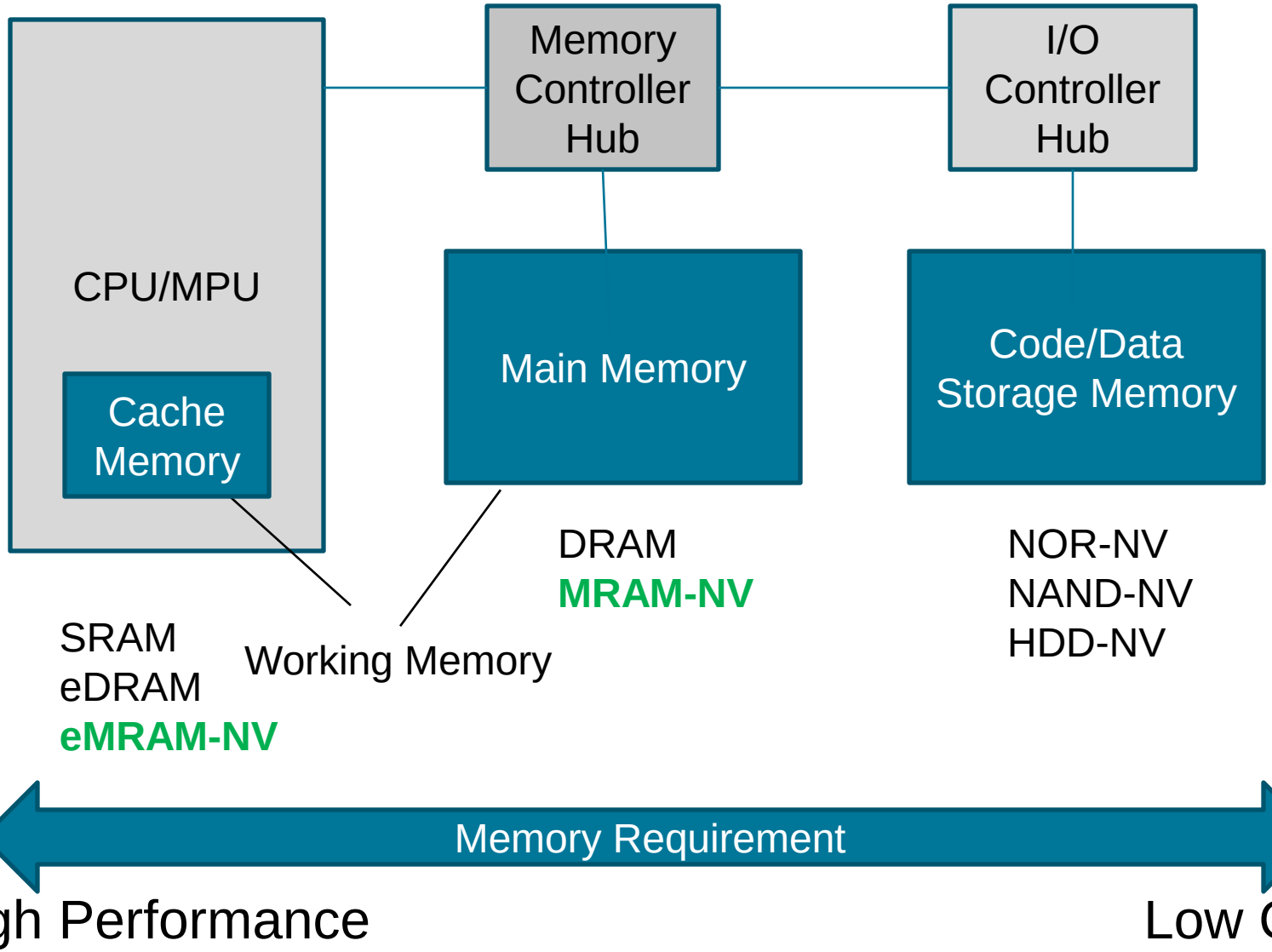
- Simple 1 transistor + 1 MTJ memory cell
- Data stored in magnetic polarization, not charge
- State of bit detected as change in resistance
- Always non-volatile
- Non-destructive read, unlimited endurance
- Leverage CMOS semiconductor ecosystem
- Everspin - “Electron spin is forever”



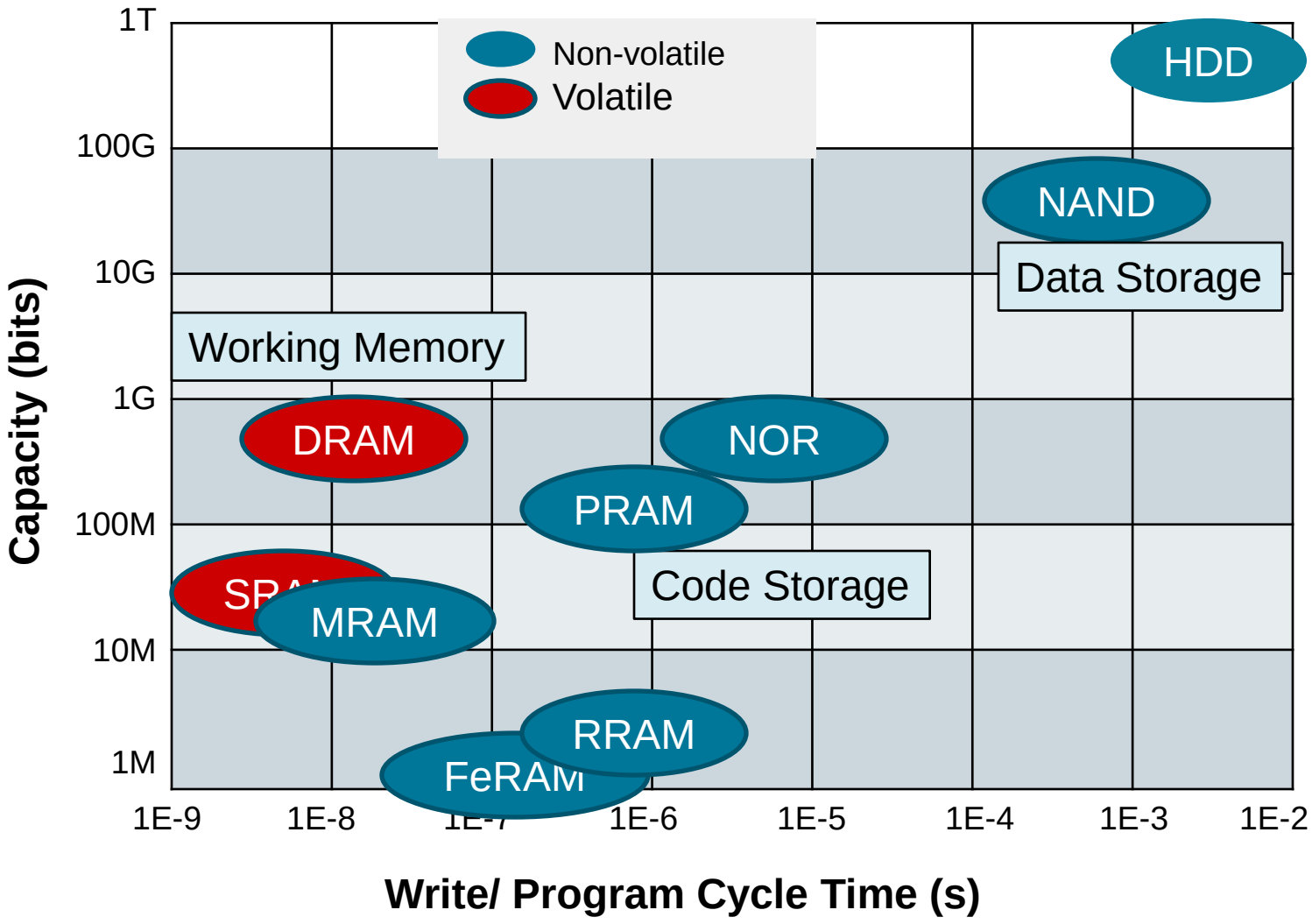
Everspin MRAM Advantages

Parameter	Capability
Non-volatile capability	• Data retention >20 years
Performance	• Symmetric read/write – 35ns
Endurance	• Unlimited cycling endurance
CMOS integration	• Easily integrates in manufacturing back-end • Compatible with embedded designs • No impact on CMOS device performance
Temperature range, reliability	• -40ºC < T < 150ºC operation demonstrated • Intrinsic reliability > 20 years lifetime at 125ºC
Soft error immunity	• MRAM cell radiation tolerant • Soft error rate from alpha radiation too low to measure (<0.1 FIT/Mb)
Environmentally friendly	• No battery, RoHS compliant, low power

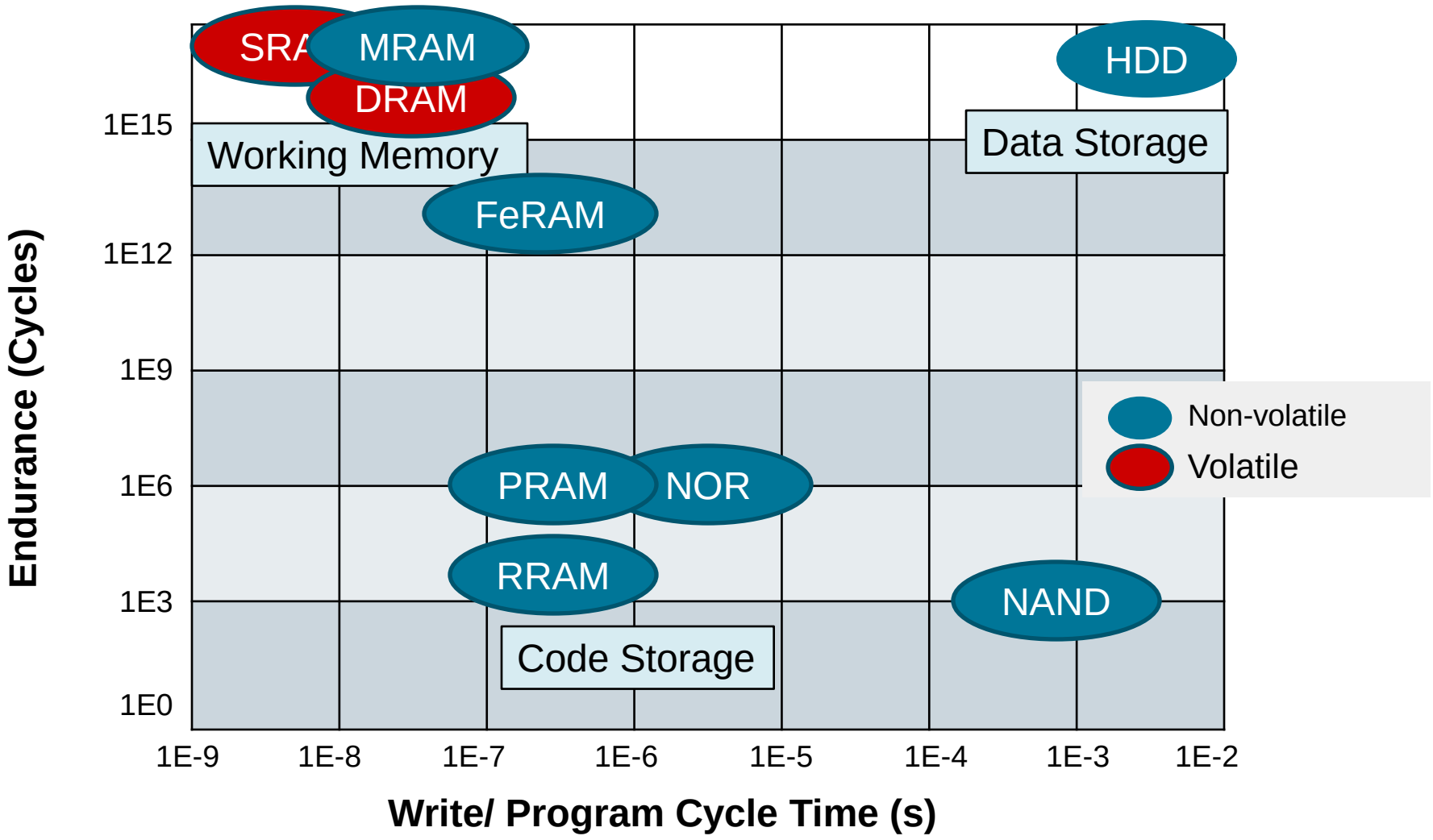
Memory System Hierarchy



Memory Capacity vs. Cycle Time



Memory Endurance vs. Cycle Time

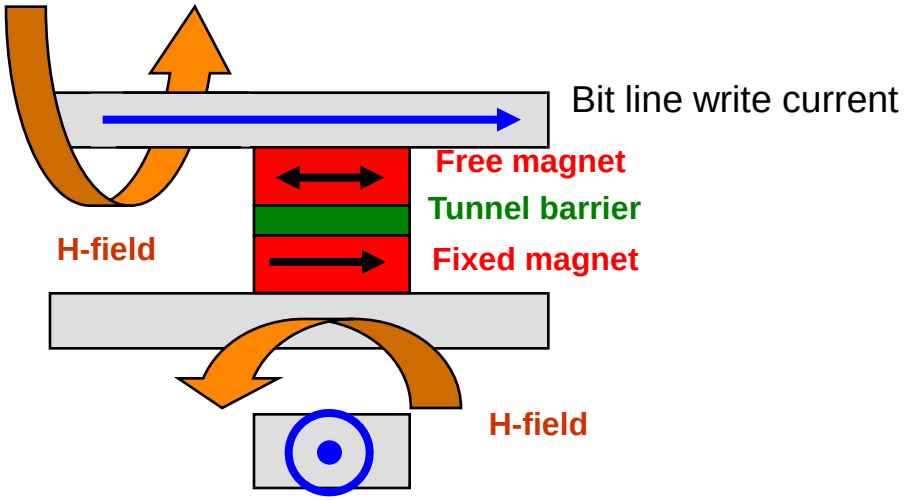


Agenda

- Current status of MRAM products
- MRAM features
- **Current MRAM product operation**
- Recent advancement in MRAM technology
- Prospect for MRAM

MRAM Writes and Reads

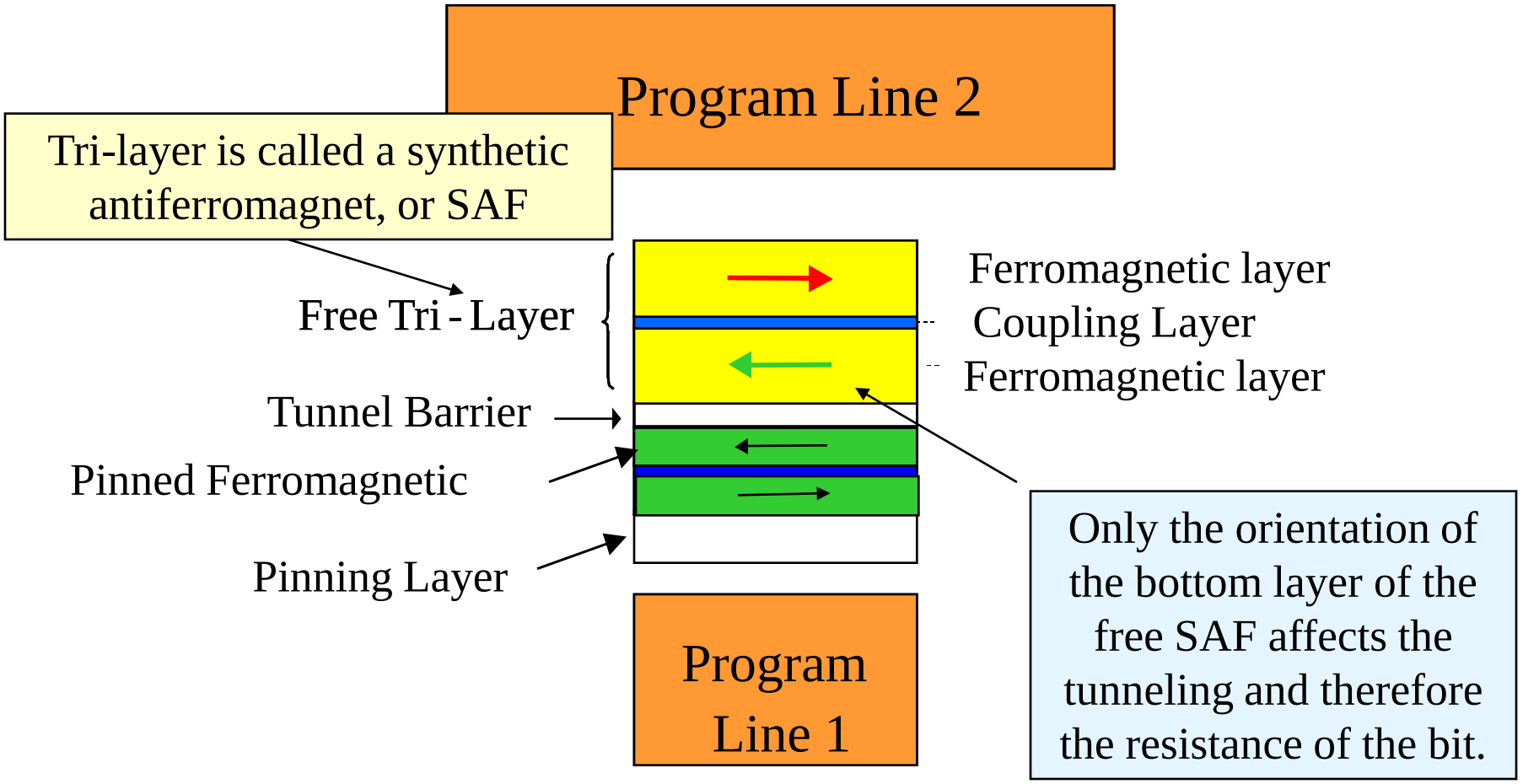
Toggle-MRAM in production



- Cross-point architecture
- Current along bit line and digit line to switch at intersection

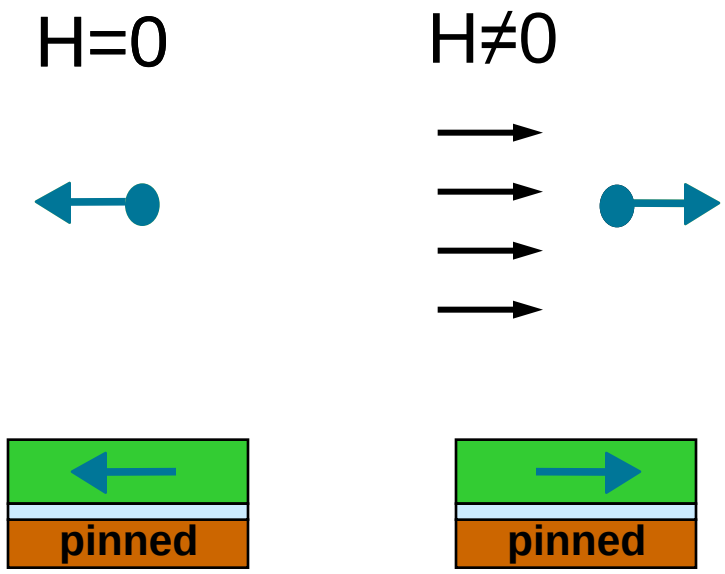
- Write Current Flows Down Write Line 1 & 2
- Magnetic Tunnel Junction (MTJ) At Cross-Point Is Polarized
- Polarization State Is Read By Selecting Pass Transistor to Sense Resistance of Specific MTJ

Toggle MRAM Bit Cell



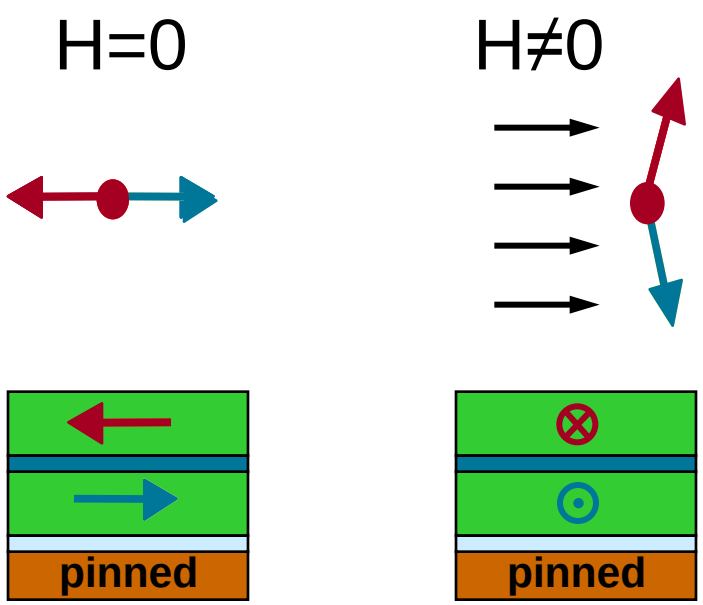
Free Layer Field Response

Conventional MRAM
Single Layer



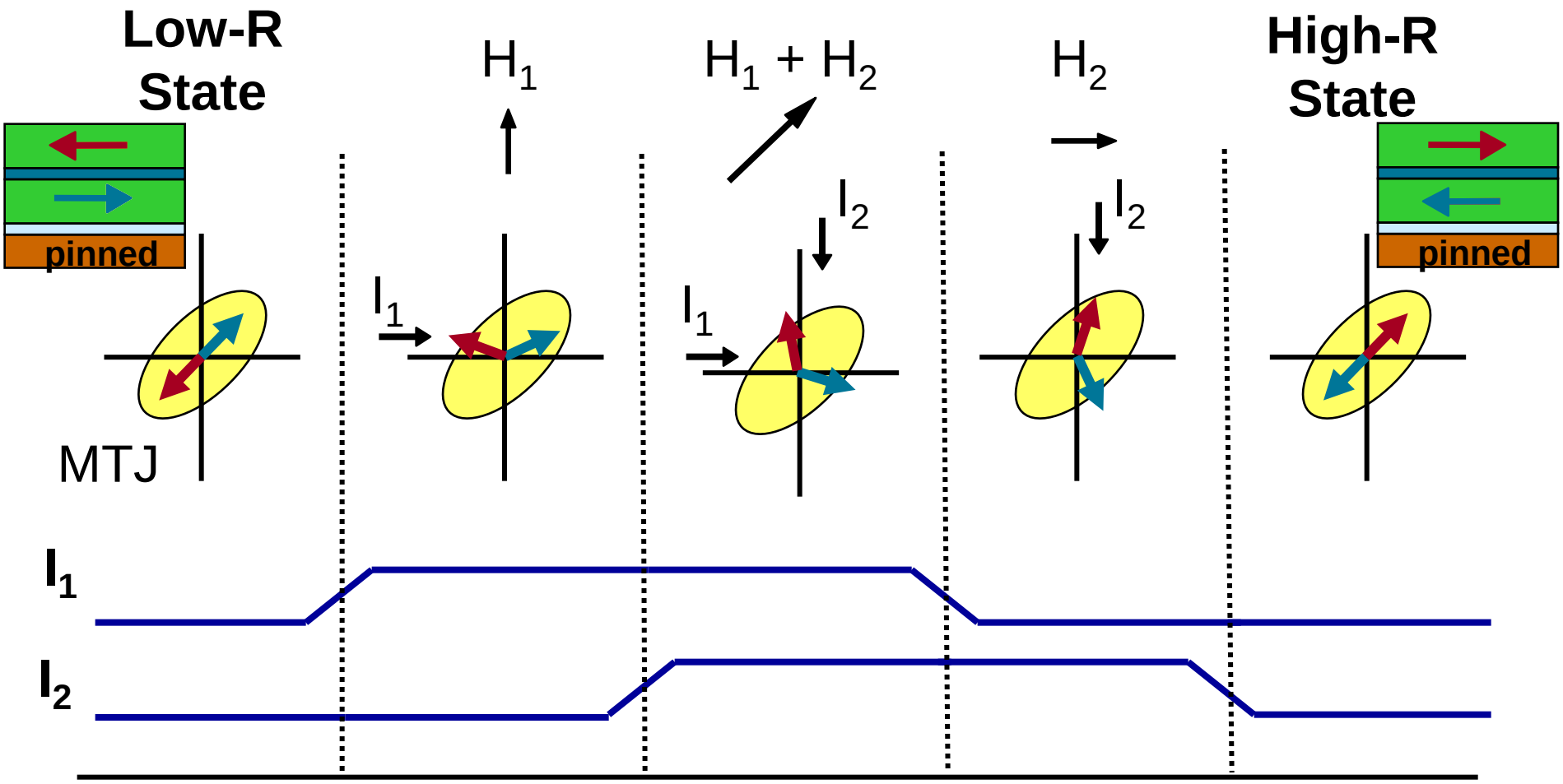
Aligns with applied field

Toggle MRAM
Coupled Trilayer



Rotates perpendicular to applied field

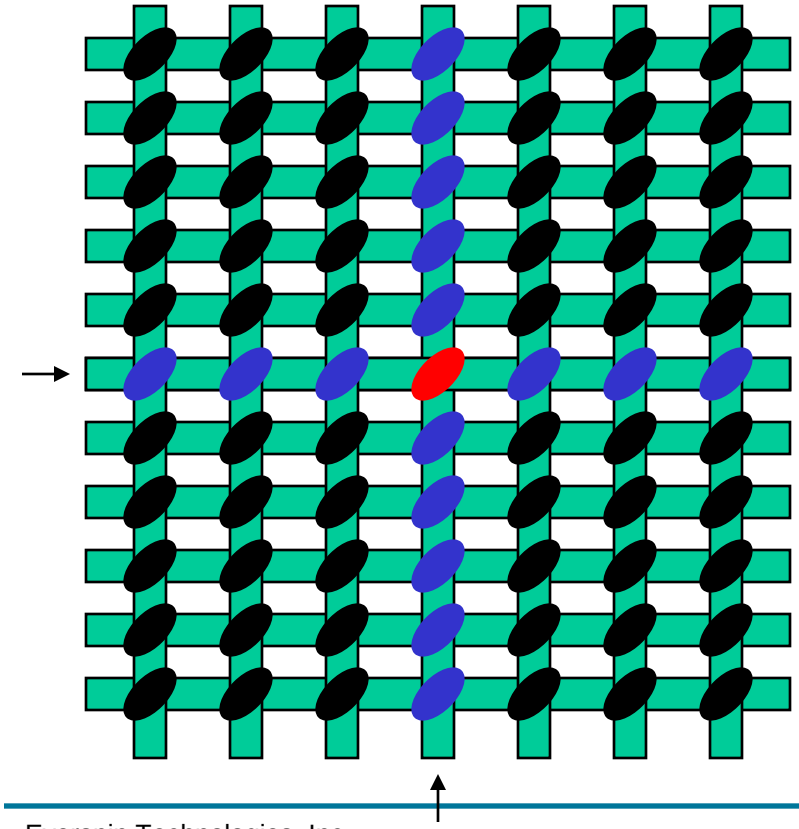
Toggle Write Operation



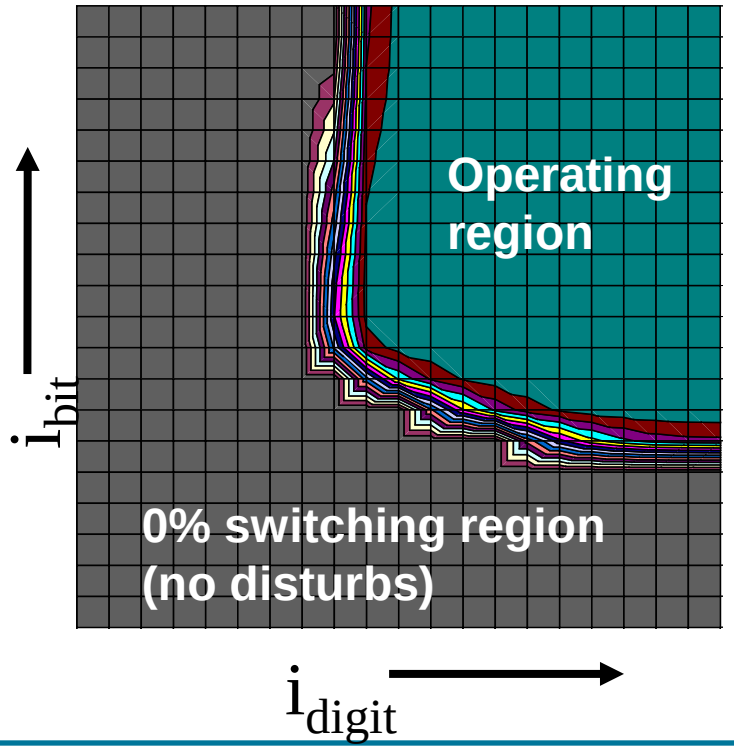
Advantages: Eliminates disturb - Large operating window

Toggle-Bit Selection

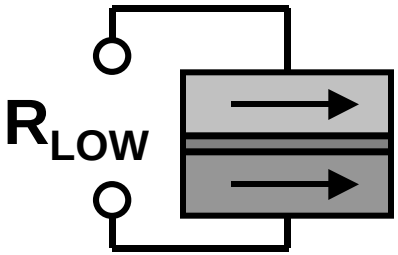
- No ½-select bit disturb
- All bits along ½-selected current lines have increased energy barrier during programming
- Single write line can not switch bits



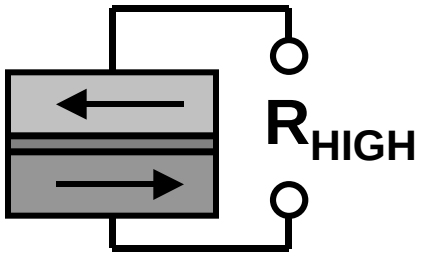
4Mb, March6N Toggle Map



MRAM Storage Concept



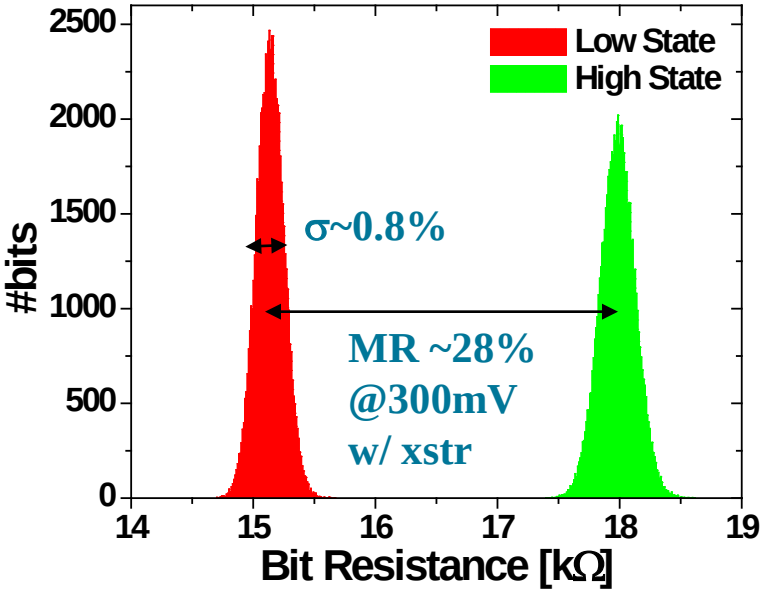
Free Layer
Tunnel Barrier
Fixed Layer

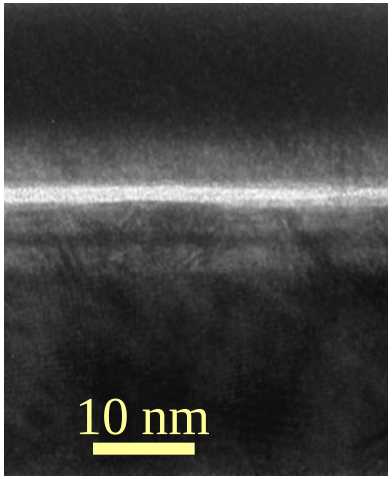


Parallel = Low Resistance

Anti-Parallel = High Resistance

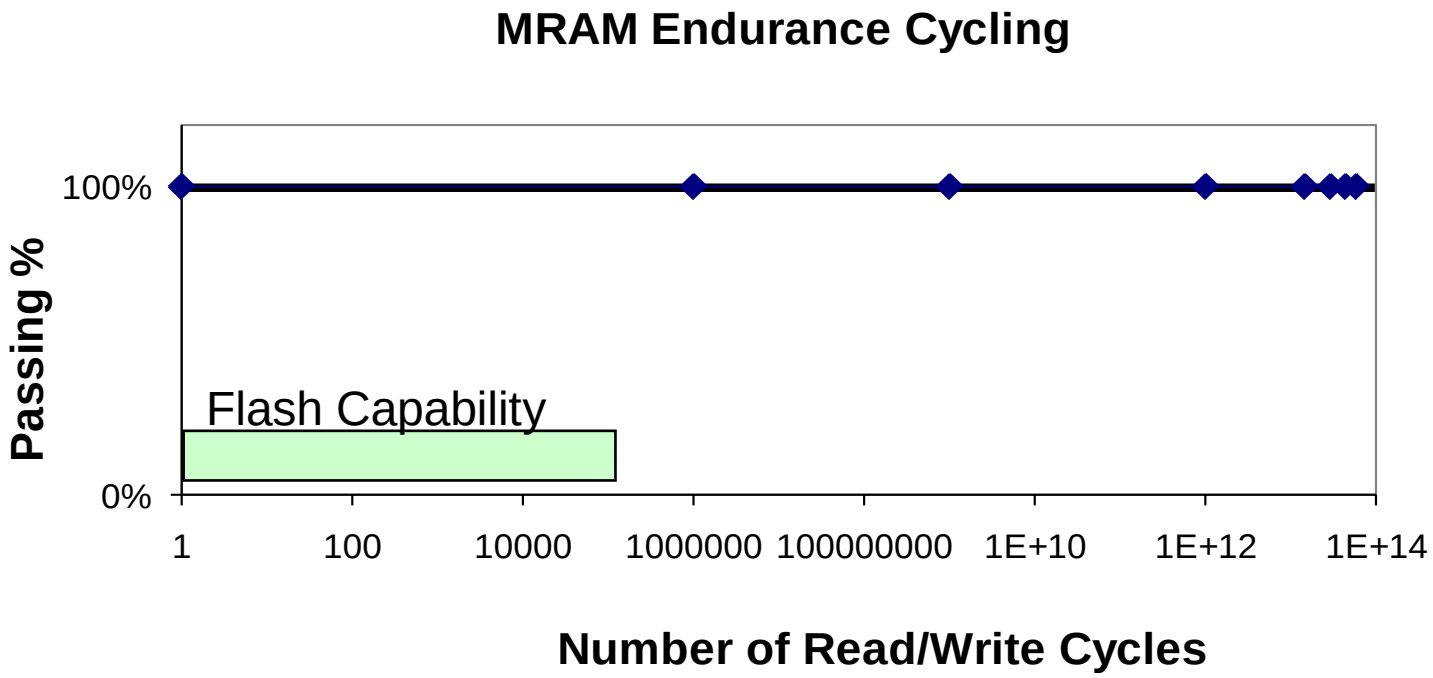
4Mb Measured Resistance Distribution





NiFe/AlOx/NiFe

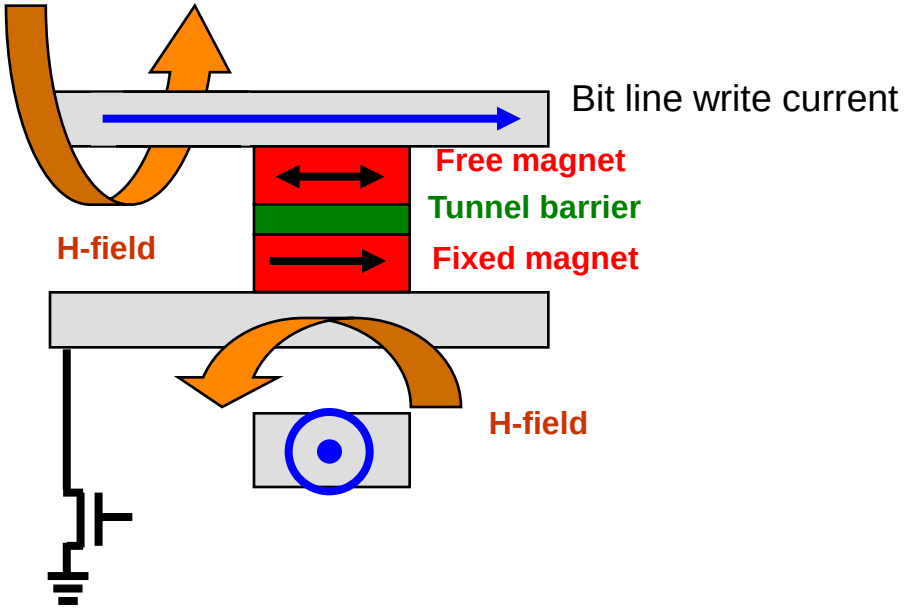
MRAM: Unlimited Read/Write Endurance



- MRAM Endurance Tested to 58 Trillion Cycles with No Change in Critical Parameters.
- Data from >2800 bits from 900 devices
- 8 orders of magnitude more cycles than current Flash technology
- No known failure modes are seen or expected

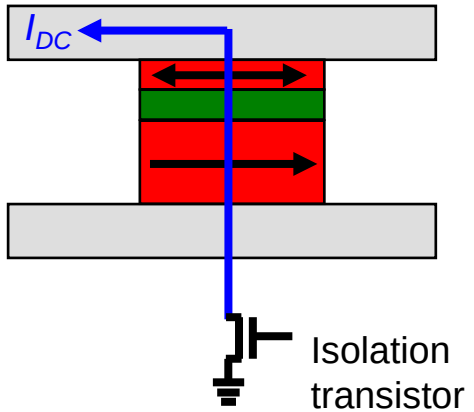
MRAM bit switching

Toggle-MRAM
in production



- Cross-point architecture
- Current along bit line and digit line to switch at intersection

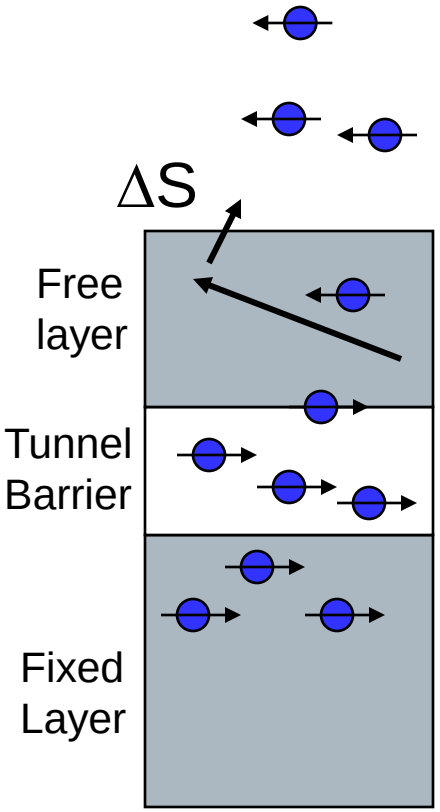
ST-MRAM
in development

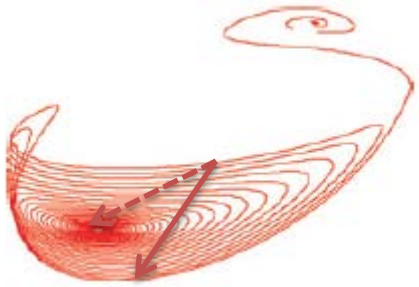


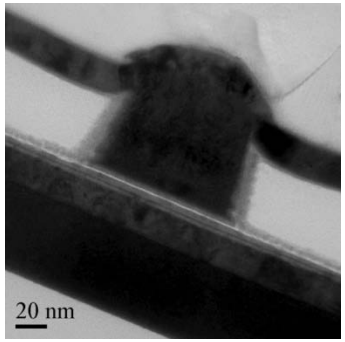
- Current I_{DC} flows through MTJ and transistor
- Fixed magnet polarizes I_{DC}
- Spin-transfer torque programs free magnet
  - Conservation of angular momentum

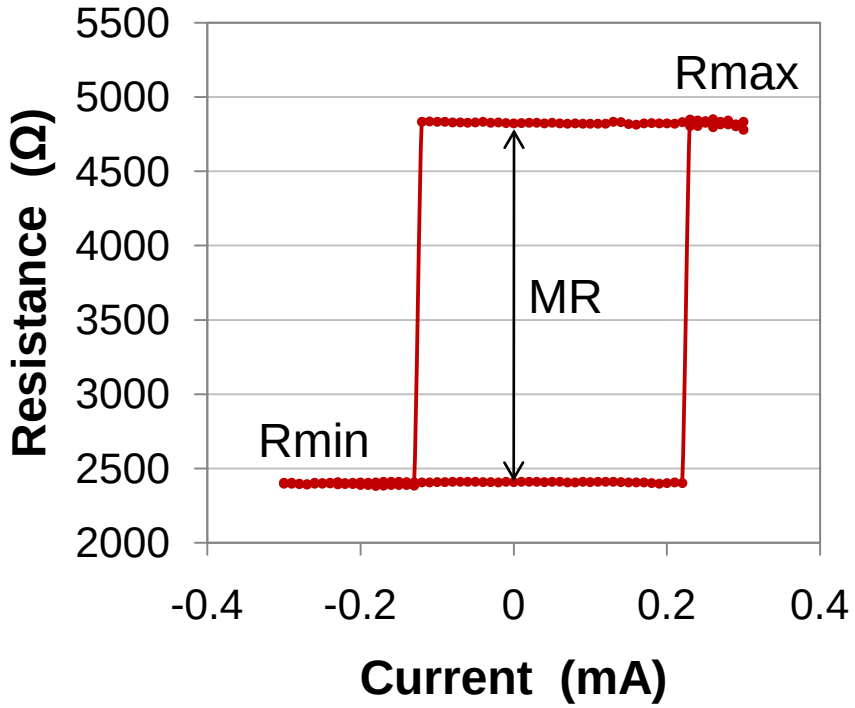
Spin Torque MRAM

Use spin momentum from current to change direction of *S*, *m*.



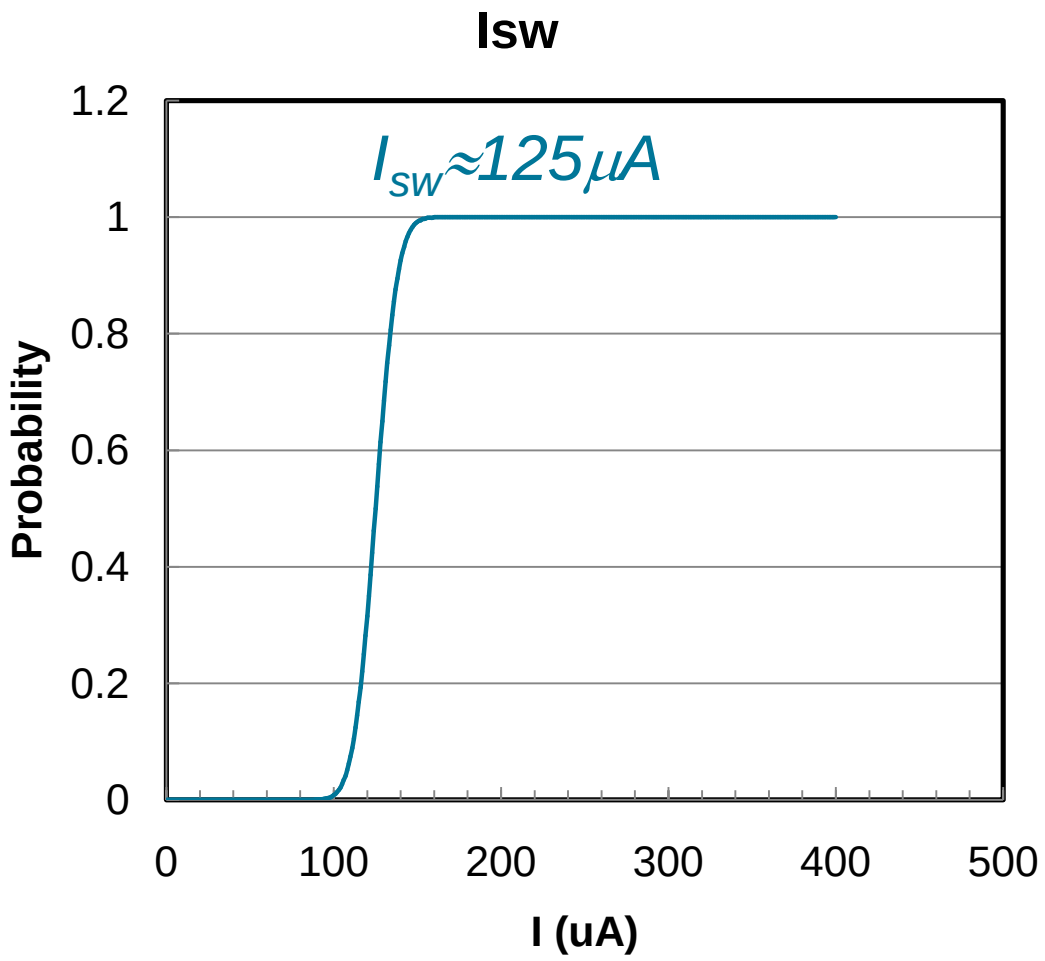






$$\frac{\Delta S}{\Delta t} = Torque$$

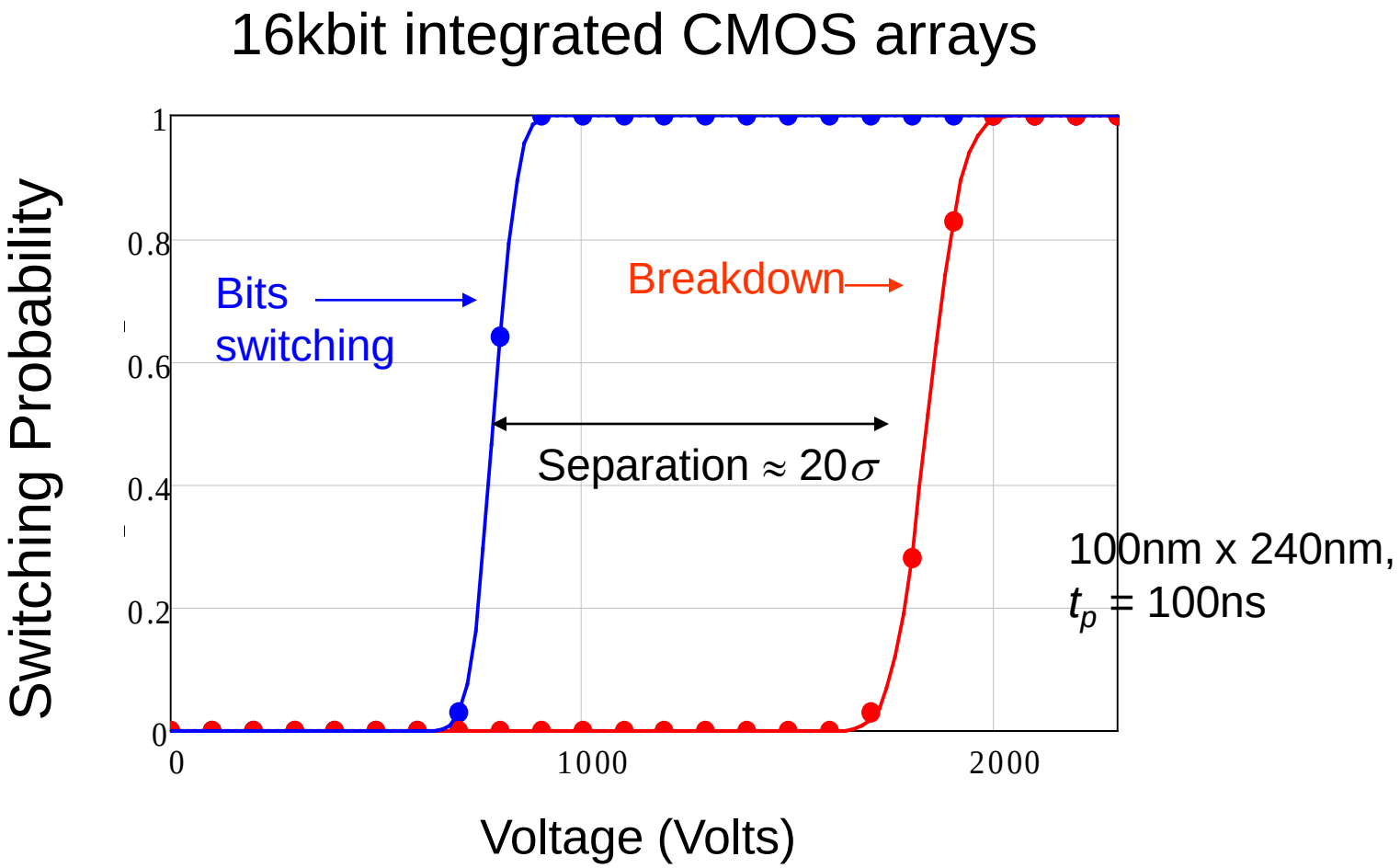
Low Switching Current



- **Demonstration of low write current with 60nm bits**
- **Energy barrier = 60kT**

Measured on 16kb CMOS array at t_p = 100ns

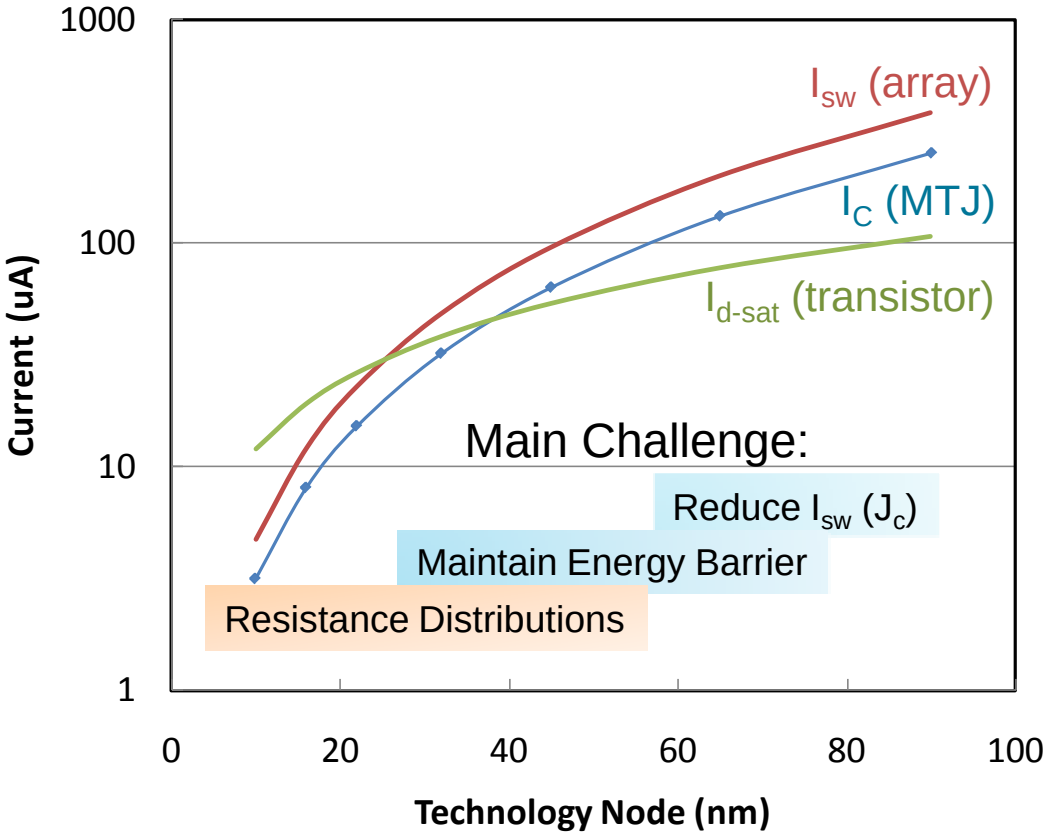
Large Separation of V_{sw} and V_{bd}



- Excellent separation ≈ 20σ, due in part to $\sigma_{sw} \approx \sigma_{bd} \approx 4\%$

Scaling ST-MRAM

- **Today: Reduce J_c for reliability and smaller transistors**
- **Continued scaling: maintain energy barrier and manage resistance distributions**



- ST-MRAM bits scale favorably to available current from transistor
  - Low Jc for reliability is the bigger issue
- Continued scaling requires innovative magnetic devices and materials
  - Enhanced energy barrier
  - Increased TMR

I_c calculated for J_c=2MA/cm^2

Memory comparison

	Toggle MRAM (180 nm)	Toggle MRAM (65 nm)*	ST MRAM (65 nm)*	FLASH (65 nm)+	DRAM (65 nm)+	SRAM (65 nm)+
cell size (μm^2)	1.25	0.16	0.04†	0.04	0.03	0.3
Read time (ns)	35	10	10	10 - 50	10	1
Program time	5 ns	5 ns	10 ns	0.1-100 ms	10 ns	1 ns
Program energy/bit	150 pJ	100 pJ	1 pJ	10 nJ	5 pJ Needs refresh	5 pJ
Endurance	$> 10^{15}$	$> 10^{15}$	$>10^{15}$	$> 10^{15}$ read, $> 10^5$ write	$> 10^{15}$	$> 10^{15}$
Non-volatility	YES	YES	YES	YES	NO	NO

* 65nm MRAM values are projected
\+ These values are from the ITRS roadmap
† This cell size only considers bit area and ignores CMOS limitations

Summary

- MRAM is a highly reliable, high-performance, nonvolatile memory ICs, with unlimited endurance
- MRAM has the unique characteristics of a working memory while providing non-volatility
- Current MRAM product densities ranges from 256kb-16Mb
- Continuous advancement in the technology would allow MRAM to drive to higher densities while maintaining its unique characteristics